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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,880	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,14 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,14 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 24, 27, 30, and 34 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The aforementioned claims include the limitation that the signals are transmitted by wireless communication. However, the independent claims from which the aforementioned claims respectively depend include the limitation that the signals are transmitted on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. A bus, by definition, is a set of hardware lines used for data transfer among the components of a computer system (See 'bus' in The Microsoft Computer Dictionary, 3rd Edition and 'bus' and 'hardware' in The Free On-Line Dictionary of Computing). Wireless, by definition, is communications taking place without the use of interconnecting wires or cables (See 'wireless' in The Microsoft Computer Dictionary, 3rd Edition and 'wireless' in The Free On-Line Dictionary of Computing). Because the signals are transmitted on an SBD bus having ternary logic levels, the signals are transmitted on a set of hardware lines and therefore cannot be transmitted wirelessly. The device as claimed is inoperative as it claims a communications medium that is both constructed of hardware lines and is wireless.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5, 9, 13, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The aforementioned claims include the limitation that the signals are transmitted by wireless communication. However, the independent claims from which the aforementioned claims respectively depend include the limitation that the signals are transmitted on a simultaneous bi-directional (SBD) memory bus having ternary logic levels. A bus, by definition, is a set of hardware lines used for data transfer among the components of a computer system (See 'bus' in The Microsoft Computer Dictionary, 3rd Edition, and 'bus' and 'hardware' in The Free On-Line Dictionary of Computing). Wireless, by definition, is communications taking place without the use of interconnecting wires or cables (See 'wireless' in The Microsoft Computer Dictionary, 3rd Edition and 'wireless' in The Free On-Line Dictionary of Computing). Because the signals are transmitted on an SBD bus having ternary logic levels, the signals are

transmitted on a set of hardware lines and therefore cannot be transmitted wirelessly. One of ordinary skill in the art would not have been able to construct a bus that is both constructed of hardware lines and is wireless.

5. Claims 32-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 20-22 are further rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 20-22 recite the limitation of "a machine readable medium having stored thereon data representing sets of instructions" which are executed by a machine. These software claims are not described in either the specification or the drawings.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 6, 14, and 23-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 1, 6, 14, and 32 and their dependant claims recite the limitation "the plurality of echoed signals" or a similar limitation. There is insufficient antecedent basis for this limitation in the claim. The claims provide for observing, reading, and echoing the signals in the alternative. Thus, echoing the signals is not a required limitation. Therefore, the limitation of "the plurality of echoed signals" is indefinite, as signals are not required to be echoed in order to be encompassed by the claims.

9. Claims 1, 6, 14, and 32 recite the limitation of "...unintrusively observing, reading, and echoing..." or a similar limitation. It is unclear if only the observing is performed unobtrusively, or if each of the observing, reading, and echoing are performed unobtrusively.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the Applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

Applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 6, 14, and 23-35 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,601,196 to Dabral et al. ("Dabral")

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

12. In reference to Claim 1, Dabral discloses an apparatus comprising a buffer having a trigger, the buffer coupled with a component further coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), the trigger to facilitate one or more of unintrusively observing and echoing of one or more of a plurality of signals transmitted on the SBD memory bus (See Column 1 Lines 50-55 and Column 3 Lines 7-10), wherein the trigger to instruct the buffer via a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is

used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would include address signals. Dabral further discloses a diagnostic device coupled with the buffer, the diagnostic device to facilitate detecting, accessing, and reading of the plurality of echoed signals (See Figure 2 Number 290 and Column 3 Lines 4-14); and an observability port coupled with the buffer, the observability port to receive the echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), wherein the observability port comprises a logic observability port (See Column 3 Lines 10-14).

13. In reference to Claim 6, Dabral discloses a method comprising transmitting a plurality of signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Column 3 Lines 15-18); unintrusively observing and echoing of one or more of the plurality of signals transmitted on the SBD memory bus via a trigger (See Column 1 Lines 50-55 and Column 3 Lines 7-10), the SBD bus coupled with a component further coupled with a buffer having the trigger (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), wherein the trigger to instruct the buffer using a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and

as such would include address signals. Dabral further discloses detecting, accessing, and reading of the plurality of echoed signals via a diagnostic device coupled with the buffer (See Figure 2 Number 290 and Column 3 Lines 4-14); and receiving the plurality of echoed signals via an observability port (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), wherein the observability port includes a logic observability port (See Column 3 Lines 10-14).

14. In reference to Claim 14, Dabral discloses a system comprising: a memory coupled with a microprocessor (See Column 1 Lines 12-14); the microprocessor coupled with a buffer having a trigger, the buffer coupled with a component further coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), the trigger to facilitate unintrusively observing and echoing of a plurality of signals transmitted on the SBD memory bus (See Column 1 Lines 50-55 and Column 3 Lines 7-10), wherein the trigger to instruct the buffer via a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would include address signals. Dabral further discloses a diagnostic device coupled with the buffer, the diagnostic device to facilitate detecting, accessing, and reading of the plurality of echoed signals

(See Figure 2 Number 290 and Column 3 Lines 4-14); and an observability port coupled with the buffer, the observability port to receive the echoed signals (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10); wherein the observability port comprises a logic observability port (See Column 3 Lines 10-14).

15. In reference to Claim 23, Dabral discloses the limitations as applied to Claim 14 above. Dabral further discloses that the diagnostic device is one of a logic analyzer and a bus analyzer (See Column 3 Lines 10-14), the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port (See Figure 2 Numbers 291 and 292).

16. In reference to Claim 25, Dabral discloses the limitations as applied to Claim 14 above. The transitional term "comprise" is inclusive or open-ended and does not exclude additional, unrecited frequencies for the echo signals (MPEP 2111.03). Because Dabral is operable to echo signals of all frequencies, it inherently echoes signals between 5GHz and 500 GHz.

17. In reference to Claim 26, Dabral discloses the limitations as applied to Claim 1 above. Dabral further discloses that the diagnostic device is one of a logic analyzer and a bus analyzer (See Column 3 Lines 10-14), the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port (See Figure 2 Numbers 291 and 292).

18. In reference to Claim 28, Dabral discloses the limitations as applied to Claim 1 above. The transitional term "comprise" is inclusive or open-ended and does not exclude additional, unrecited frequencies for the echo signals (MPEP 2111.03). Because Dabral is operable to echo signals of all frequencies, it inherently echoes signals between 5GHz and 500 GHz.

19. In reference to Claim 29, Dabral discloses the limitations as applied to Claim 6 above. Dabral further discloses that the diagnostic device is one of a logic analyzer and a bus analyzer (See Column 3 Lines 10-14), the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port (See Figure 2 Numbers 291 and 292).

20. In reference to Claim 31, Dabral discloses the limitations as applied to Claim 6 above. The transitional term "comprise" is inclusive or open-ended and does not exclude additional, unrecited frequencies for the echo signals (MPEP 2111.03). Because Dabral is operable to echo signals of all frequencies, it inherently echoes signals between 5GHz and 500 GHz.

21. In reference to Claim 32, Dabral discloses transmitting a plurality of signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels (See Column 3 Lines 15-18); unintrusively observing and echoing of one or more of the

plurality of signals transmitted on the SBD memory bus via a trigger (See Column 1 Lines 50-55 and Column 3 Lines 7-10), the SBD bus coupled with a component further coupled with a buffer having the trigger (See Figure 2 Number 250, Column 1 Lines 12-14, and Column 3 Lines 15-18), wherein the trigger to instruct the buffer using a control signal based indication (See Column 1 Lines 14-17 and Column 3 Lines 7-10), and a time-based indication (See Column 1 Lines 14-17). The trigger of Dabral will inherently instruct the buffer using an address-signal based indication, as the device of Dabral is used in a system for transferring data between devices that include processors, storage devices, and I/O devices (See Column 1 Lines 12-14), and as such would include address signals. Dabral further discloses detecting, accessing, and reading of the plurality of echoed signals via a diagnostic device coupled with the buffer (See Figure 2 Number 290 and Column 3 Lines 4-14); and receiving the plurality of echoed signals via an observability port (See Figure 2 Numbers 258 and 259 and Column 3 Lines 7-10), wherein the observability port includes a logic observability port (See Column 3 Lines 10-14).

22. In reference to Claim 33, Dabral discloses the limitations as applied to Claim 32 above. Dabral further discloses that the diagnostic device is one of a logic analyzer and a bus analyzer (See Column 3 Lines 10-14), the diagnostic device coupled to an observability bus, the observability bus further coupled to the observability port (See Figure 2 Numbers 291 and 292).

23. In reference to Claim 35, Dabral discloses the limitations as applied to Claim 32 above. The transitional term "comprise" is inclusive or open-ended and does not exclude additional, unrecited frequencies for the echo signals (MPEP 2111.03). Because Dabral is operable to echo signals of all frequencies, it inherently echoes signals between 5GHz and 500 GHz.

Response to Arguments

24. Applicant's arguments with respect to claims 1, 6, 14, and 23-35 have been considered but are moot in view of the new ground(s) of rejection.

25. In response to Applicant's arguments that Dabral has been removed as a reference under 35 USC §102(e) due to the statement of common ownership, the Examiner notes that the text of 35 USC §103(c), which Applicant is relying upon, states "Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under ***this section*** where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person." (35 USC §103(c); emphasis added). The section referred to is the section to which 35 USC §103(c) falls under; namely, 35 USC §103. A statement under 35 USC §103(c) is effective for disqualifying a reference used in a rejection under 35 USC §103(a) when the reference, due to its

filing date, constitutes prior art only under 35 USC §102(e). It is not effective for disqualifying a reference used in a rejection under 35 USC §102(e). As previously stated, a rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131. As Dabral was only used in rejections under 35 USC §102(e), and not under 35 USC §103(a), the statement does not remove Dabral as a reference under 35 USC §102(e) against the claims of the current application.

26. In response the Applicant's argument that neither La Joie, Tanaka, Gonzales, Yamamoto, or Assouad teach one or more of unintrusively observing, reading, and echoing of one or more of the plurality of signals, the Examiner will interpret "unintrusively" as defined in the specification: "without disturbing electrical properties of the bus, without adding bus latency, and without adding signal discontinuities."

Conclusion

27. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US Patent Number 5,801,549 to Cao et al.; US Patent Number 6,704,277 to Dabral et al.; US Patent Number 5,604,450 to Borkar et al.; US

Patent Number 6,128,754 to Graeve et al.; US Patent Number 6,661,303 to Ghoshal et al.; and "A 900 Mb/s Bidirectional Signaling Scheme" by Mooney et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cottingham can be reached on 571-272-7079. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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